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(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211(JP)

(72) Inventor: Ogawa, Junji
8-17-207, Minamisenzoku 1-chome
Ota-ku Tokyo 145(JP)

(74) Representative: Billington, Lawrence Emlyn et al,
HASELTINE LAKE & CO Hazlitt House 28 Southampton
Buildings Chancery Lane
London WC2A 1AT(GB)

(54) **Semiconductor memory device.**

(57) An identification system to identify objects from a remote interrogation station is used with moving objects such as railroad cars. The system remotely programs and stores information on an object and remotely retrieves information from the object. An information and identity storage device (10) is located on the object and at least one interrogation station (11) is located remotely from the object.

Fig. 7

Fig. 7A | Fig. 7B | Fig. 7C

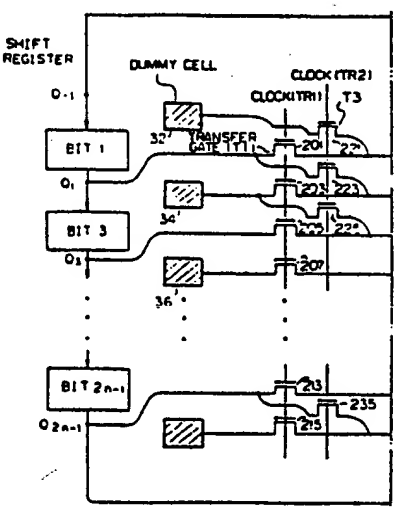

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Fig.7B

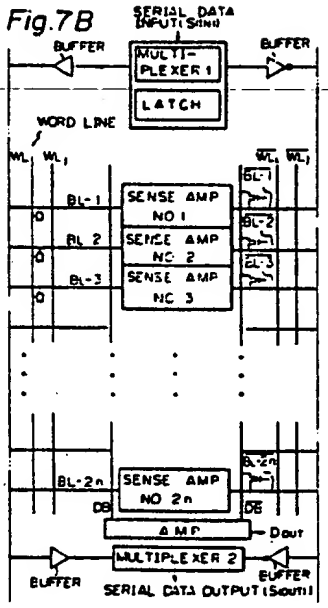
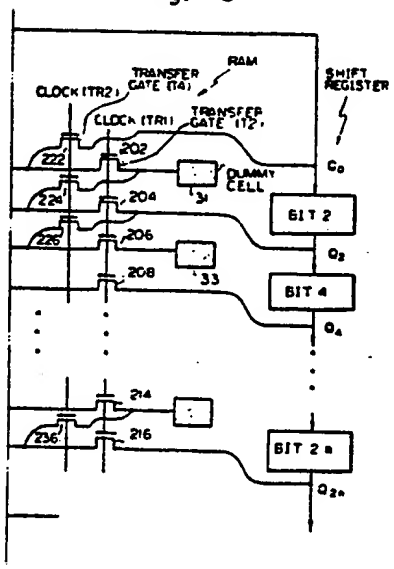

SERIAL DATA INPUT (Sin)
BUFFER
MULTI-PLEXER 1
LATCH
BUFFER
WORD LINE
WL0
WL1
BL-1
BL 2
BL-3
SENSE AMP NO 1
SENSE AMP NO 2
SENSE AMP NO 3
BL-2n
SENSE AMP NO 2n
DB
AMP
Dout
MULTIPLEXER 2
BUFFER
BUFFER
SERIAL DATA OUTPUT (Sout)

Fig.7C


RAM
TRANSFER GATE (T4)
CLOCK (TR2)
CLOCK (TR1)
TRANSFER GATE (T2)
SHIFT REGISTER
222
202
DUMMY CELL
224
204
BIT 2
226
206
208
BIT 4
214
236
216
BIT 2n

SEMICONDUCTOR MEMORY DEVICE

0178922

The present invention relates to a semiconductor memory device having a built-in high-speed read/write shift register of a capacity corresponding to a group of memory cells on a word line, more particularly to a device directed to enabling one-bit shift in write transfer operations and driving a divided shift register.

In the related art, there are known semiconductor memory devices which have a random access memory (RAM) and a shift register that can parallel-transfer data of a group of memory cells on a word line, thus enabling high-speed read/write operations. The semiconductor memory devices are utilized advantageously for image processing and the like, e.g., for use as video RAM's (VRAM's).

In one prior art VRAM, stages of a shift register are arranged in two columns; one for odd number bit lines and one for even number bit lines. An input side multiplexer allots serial data input S(in) alternately to the odd column and even column bit by bit. An output side multiplexer combines the odd column output and the even column output to form serial data output. Internal clocks, equivalent to one cycle of a shift clock, are used. Thus, two cycles of a shift a clock are needed for a one-bit shift in the two columns. On the other hand, changes in the output data after combination by the output multiplexer correspond to one cycle of the shift clock.

Thus, the rate of data transfer in the odd column and the even column is one-half that of the external input data and the external output data. This means a low-speed shift register will do. Alternatively, if the shift register is used as a basis, it is possible

to double the bit rate of the external input/output data and, thus, to achieve high-speed RAM write/read operations.

In the odd and even shift register columns, since two cycles of a shift clock are used for a bit shift, if a parallel data write-in operation is performed on a RAM for each cycle of the shift clock, then, while a prior stage of data (Q_{N-1}) is in a master stage, the output (Q_N) of the slave stage will be transferred to the RAM even if the output is the same as before or if the slave stage is in the process of change the output is still not settled.

It has been conceived to parallel transfer data to the RAM after the completion of a shift operations. In this case, there is the problem that the odd column can only be connected to odd number bit lines, and the even column can only be connected to even number bit lines. Due to this, a two-bit shift can be executed, but not a one-bit shift. If parallel data transfer were performed per each shift clock, e.g., if word line selection were performed in the order n-th, (n+1)-th, (n+2)-th, and so on, the display screen of the apparatus incorporating the VRAM would show the same pattern horizontal lines shifted by one bit. This type of processing may sometimes be required for image processing, but division of a shift regieter into odd number stages and even number stages would, again, limit such processing to two-bit units.

It is accordingly desirable to provide an improved semiconductor memory device with a high-speed read/write shift register, having a capacity corresponding to a memory cell group connected to one word line, which enables one-bit-shift writing for a plurality of shift register columns.

According to an embodiment of the present invention, there is provided a semiconductor memory device including: a RAM

portion; a shift register for enabling parallel transfer of a one word line amount of data of the RAM portion between the RAM portion and the shift register, the shift register being divided into a plurality of shift register portions, serial input data being distributed alternately between the shift register portions by the operation of a multiplexer, serial output data being obtained by picking up data alternately from the shift register portions by the operation of another multiplexer; a transfer gate portion inserted between the RAM portion and the shift register for carrying out parallel transfer, the transfer gate portion consisting of a plurality of groups of transfer gates for enabling selective connections of input and output terminals of each of stages of the shift register portions with either of the adjacent odd number bit line and even number bit line of the RAM portion, the plurality of transfer gate groups being switched in correspondence with shift clock signals.

In parallel data transfer from the shift register to the RAM, when a slave clock occurs, each stage of the slave output is post-shift data, so the output is written into the RAM as it is. When a master clock occurs, each stage of the slave output is pre-shift data, so the transfer gate is operated and the output is written into the following bit line. This enables one-bit shifts. Also, the odd and even columns of the shift register can be coupled with either odd or even number bit lines.

Figure 1 is a schematic block diagram of a prior art VRAM;

Fig. 2 is a circuit diagram of a shift register stage having a master and slave constitution;

Fig. 3 shows waveforms of the shift operation of the VRAM;

Fig. 4 is a schematic block diagram of a prior art dynamic RAM in a normal mode;

Fig. 5 shows waveforms of the shift operation of the VRAM;

Fig. 6 is a view explaining a bad shift in the VRAM in Fig. 3;

Fig. 7 is a view of an embodiment of the present invention;

Fig. 8 is a view of another embodiment of the present invention;

Fig. 9 shows waveforms for explaining (a) transfer from a RAM to a shift register and (b) transfer from a shift register to a RAM; and

Fig. 10 is a view of yet another embodiment of the present invention.

Before entering into the description of the preferred embodiments, examples of prior art VRAM devices will be described. Figure 1 is a schematic view of an example of a VRAM. In the Figure, 1 is a shift register and 101 to 108 are stages (bits) of the same. The RAM, a dynamic RAM in this example, has eight pairs of bit lines BL-1, $\overline{\text{BL-1}}$ to BL-8, $\overline{\text{BL-8}}$, so there are eight memory cells on a word line (in practice, more memory cells are generally provided). Therefore, eight stages are used for the shift register. The RAM has sense amplifier Nos. 1 to No. 8 arranged in the center. The pairs of bit lines BL-1, $\overline{\text{BL-1}}$ to BL-8, $\overline{\text{BL-8}}$ are connected thereto from the two ends. A plurality of word lines are arranged to intersect with these bit lines. Memory cells 41 to 48 are connected to the bit lines and word lines. A first group of transfer gates (T1) 201 to 208 are connected to the shift register 1 and the sense amplifier Nos. 1 to No. 8, and a second group of transfer gates (T2) 209 to 216 are connected to the sense amplifier Nos. 1 to No. 8 and dummy cells 31 to 38. The dummy cells are used for write transfer of the RAM. The transfer gates 201 to 216 receive parallel transfer clocks between the shift register 1 and RAM.

An example of a stage of the shift register 1 is provided in Fig. 2, showing a well-known dynamic shift register. The figure shows the shift register having a master-slave constitution an inherent feature of registers as well. In Fig. 2, prior stage output Q_{N-1} is received first in a master part composed of transistors T11 to T13. Next, the content of the master part is introduced into a slave part composed of transistors T14 to T16 to make it its own output Q_N. An operative clock P1 of the master part and an operative clock P2 of the slave part have opposite phases, as shown in Fig. 3. These are internally formed so as to correspond to the first half and second half of a cycle of an external shift clock. Accordingly, when an external clock is provided, the clocks P1 and P2 are internally formed for fetching prior stage data into the master part and transferring the data to the slave part. Each time an external clock (SCLK) is intput, a one-bit shift is reliably executed. At the bottom of Fig. 3 is shown the serial output of the shift register.

A high-speed write operation of a memory RAM is carried out as follows. Write data is sent serially bit by bit. Input data SIN is written bit by bit into a first stage SR1 of the shift register 1 in synchronization with a shift clock SCLK and consecutively transferred to the following stages SR2, SR3, ... In this example, when eight bits are written and transferred, each stage SR1 to SR8 of the shift register is filled, whereupon the transfer gates T1 and T2 are opened to carry out the write-in operation. That is, the bit lines BL-1, BL-2, ... are connected to the output terminals of the stages SR1, SR2, ... of the shift register, so when the transfer gates T1 and T2 are opened, a high-low comparison is made of the potential of each output terminal of shift register and the potential of the dummy cells 31 to 38. The potential difference is enhanced by the sense amplifiers No. 1 to

No. 8, making either of bit lines BL1 and $\overline{BL1}$, BL2 and $\overline{BL2}$, ... as H (high) and the other as L (low). In this state, when a word line WL is selected (either on BL side or $\overline{BL}$ side), all the memory cells associated with that word line are simultaneously written with the H or L level of the corresponding bit lines. In general, RAM's are written into bit by bit (memory cell). The present system improves the speed by the number of memory cells on the word line, in this case, eight-fold.

The memory cells on a word line often correspond to the horizontal picture elements of the display of the apparatus using the VRAN. In this case, the number of memory cells is equal to the number of picture elements N (for instance N=512). The number of stages of the shift register is also equal to N. When N bits of input data SIN are introduced into the shift register, they are simultaneously written into the RAM as explained above. When the following N bits are introduced into the shift register, they are again simultaneously written into the RAM. This is repeated by a number of times corresponding to the number of longitudinal picture elements M, for instance, M=512 to complete the writing of one screen's worth of data. The number of word lines of the RAM is equal to M.

The read-out of the RAM is carried out as follows. That is, first, all the bit lines BL-1, $\overline{BL-1}$, BL-2, ... of the RAM are precharged. A word line WL is selected, whereupon the potential of the bit lines is changed by the stored data of the memory cells associated with the word line. The differences between the potentials of these bit lines and the potentials of the bits lines connected with dummy cells (not shown) are enhanced by sense amplifiers. The thus difined H and L levels of the bit lines (BL-1, BL-2, ...) are input into the stages of the shift register by the opening of the transfer gate (T_1). This data is fetched out in a bit serial mode as the output data SOUT by the shift clock

SCLK. The output data SOUT becomes a video signal for a horizontal scanning line on the display.

Note that a picture element on a display is expressed genearally not by one bit, but by a plurality of bits. In this case, as shown in Fig. 1, a plurality of memory units are arranged in paralle. The shift register, except during parallel transfer (writing into a RAM and read-in therefrom), receives a serial data input signal SIN from an input terminal by a shift clock SCLK and outputs the signal from an output terminal as SOUT.

In the device of Fig. 1, the data input and transfer to the shift register 1 are carried out bit by bit. The same is true of the external serial input/output data and data transfer rate. To speed up the writing and reading of the RAM, the shift register 1 must be operated at a faster speed. This is not, however, very simple.

One idea has been to arrange the stages of the shift register in a plurality of columns. Figure 4 shows a prior art VRAM having two shift register columns one for odd number bit lines and one for even number bit lines. In the figure, SR1, SR3, SR5, SR7 are odd number shift register stages, and SR2, SR4, SR6, and SR8 are even number shift register stages. MPX1 is an input side multiplexer, which allots serial data input S(in) alternately to the odd column and even column bit by bit. MPX2 is an output side multiplexer, which combines the odd column output and even column output to form serial data output S(OUT).

Figure 5 is an operative waveform diagram of Fig. 4. In the figure, internal clocks P1 and P2 are, respectively, to one cycle of the shift clock SCLK. Thus, two cycles of the shift clock SCLK are necessary for a one-bit shift in the two colulmns. A change in output data S(OUT) after combination by the multiplexer 2, however, corresponds to one cycle of the shift clock SCLK.

As mentioned earlier, therefore, the rate of data transfer in the odd column and even column is one-half that of the external input data S(in) and the external output data S(OUT). This, again, means a low speed shift register will do or, if the shift register is used as a basis, that it is possible to double the bit rate of external input/output data.

In the odd and even shift register columns, as shown in Fig. 4, two cycles of a shift clock SCLK (i.e., two clocks) are used for a bit shift, so if a parallel data write-in operation is performed on a RAM for each cycle of the shift clock SCLK, then, while a prior stage of data Q_{N-1} is in a master stage, as shown in Fig. 2, the output Q_N of the slave stage will be transferred to the RAM even if the output is the same as before or if the slave stage is in the process of change and the output is still not settled. In Fig. 1, as opposed to Fig. 4, performed without problem.

Figure 6 is a view explaining a bad shift in the VRAM of Fig. 4 in Fig. 6, "0" is input into the shift register column 2 having the serial data 11010001. When the shift by the slave stage of clock P2 is finished, the content of data in the shift register column 1 is 01101000. This is parallel transferred to the group of memory cells on the selected word line WL in the memory cell array. If, however, the shift register is divided in odd and even columns as in Fig. 4 and transfers are performed at a 1/2 bit rate, the first clock of the shift clock SCLK is the P1 stage of the master clock on the odd column shift registers and the even column. If a parallel transfer is executed in this state, the old or undecided data in the odd column and even column prior to the shift completion will be transferred to the memory side. If it is intended to carry out parallel transfer of data to the RAM after completion of the shift operation, as is apparent from the constitution of Fig. 4, the odd column can only be connected to odd

number bit lines BL1, BL3, and so on, and the even column can only be connected to even number bit lines $\overline{BL2}$, $\overline{BL4}$, and so on. Thus, while a two-bit shift can be executed, a one-bit shift cannot. If parallel data transfer were performed per each cycle of the shift clock SCLK, e.g., if word line selection were performed in the order n-th, (n+1)-th, (n+2)-th, and so on, the display screen of the apparatus incorporating the VRAM would show the same pattern horizontal lines a shifted by one bit. As mentioned before, this typing of processing may sometimes be required for image processing, but division of a shift register into odd number stages and even numbers stages would limit such processing to four bit units.

A semiconductor memory device according to an embodiment of the present invention is shown in Fig. 7. In Fig. 7, transfer gates T3 221 to 235 and T4 222 to 236 are provided. The odd column of shift register stage No. 1 to No. 7 and the even column of shift register stage No. 2 to No. 8 can be connected to the odd number bit lines (BL1, BL3, BL5, and BL7) and the even number bit lines (BL2, BL4, BL6, and BL8). Dummy cells are also connected to the odd and even number bit lines. The selection of transfer gates T1 to T4 is carried out by the exclusive transfer clocks TR1 and TR2. That is, if the clock TR2 is the L level and the clock TR1 is the H level, gates T1 and T2 turn on, just as in Fig. 4 (normal mode). If the clock TR2 is the H level, and the clock TR1 is the L level, the gates T3 and T4 turn on. Then, contrary to Fig. 4, the odd number bit lines are connected to the even column of shift register stage No. 2, No. 4, No. 6, and No. 8 and the even number bit lines are connected to the odd column of shift register stage No. 1, No. 3, No. 5, and No. 7 (inversion mode).

This inversion mode enables a one-bit shift. That is, in the inversion mode the coupling of the RAM and the shift register stages is inverted from odd to

even or vice versa. For instance, the connection of the shift register stage No. 1 and bit line BL-1, shift register stage No. 2 and bit line $\overline{BL-2}$, shift register stage No. 3 and bit line BL-3, and so on changes to connection of the shift register stage No. 1 and bit line BL-2, shift register stage No. 2 and bit line $\overline{BL-3}$, shift register stage No. 3 and bit line BL-4, and so on. Therefore, after an intermediate shift by a master stage clock (P1 in Fig. 3), if the device enters into a RAM parallel transfer write mode, the write operation is carried out in the form of BL-2=Q_1 , $\overline{BL-3}$=Q_2 , BL-4=Q_3 , and so on (where $\overline{BL-1}$=Q_0). This operation is the same as the parallel write after a one-bit shift in Fig. 1.

In the normal mode, after the data shift of Q_{-1}→Q_1 , Q_0→Q_2 , Q_1→Q_3 , ... has been finished, a write operation of Q_{-1}→bit line BL-1, Q_0→bit line BL-2, Q_1→bit line BL-3, and so on is carried out and a one-bit shift is again carried out. Thus, selection of transfer clocks TR1 and TR2 corresponding to master clocks P1 and P2 enables a one-bit shift on a RAM is enabled and prevents writing of undecided data into the RAM.

Incidentally, in Fig. 7, the odd column of shift register stage No. 1, No. 3, No. 5, and No. 7 and the even column of shift register stage No. 2, No. 4, No. 6, and No. 8 were arranged to the left and the right of the cell array, respectively, but, in practice, they may be arranged either to the left or to the right. When the transfer gates T1 to T4 are closed, the shift register and the RAM operate independently, so the shift register can be utilized to shift serial data input S-IN and serial data output S-OUT. A read/write operation of a RAM in a state separated from a shift register is generally carried out in one-bit units, as is well known, through data buses DB and $\overline{DB}$ arranged on the two sides of the group of sense amplifier No. 1 to No. 8.

The above description was made in reference to a shift register divided into two columns, but it is

apparent that the shift register can be divided into four columns, eight columns, and the like for operation at faster speeds.

Figure 10 shows an embodiment where the shift register is divided into four columns. Compared with Fig. 7, a multiplexer portion for the serial input S-IN and serial output S-OUT is omitted.

Figure 8 is a view of another embodiment of the present invention. With regards to the bit lines WLn and $\overline{WLn}$, a pair of active pull-up circuits are connected to the sense amplifier No. n. In other points, the operations of a shift register and transfer gates are the same as in Fig. 7.

Figure 9 is a view of the operation of a RAM. In the figure, in the write-in operation of a dynamic RAM, a reset signal R carries out precharging of bit lines (BL and $\overline{BL}$). For an address, the potentials of BL, $\overline{BL}$, AP (an active pull-up circuit), ø, DWL, TR1, WL1, and TDW are shown. The upper portion and lower portion express the transfer from a RAM to a shift register and the transfer from a shift register to a RAM.

CLAIM

A semiconductor memory device comprising:

a random access memory portion;

a shift register for enabling parallel transfer of a one word line amount of data of said random access memory portion between said random access memory portion and the shift register, said shift register being divided into a plurality of shift register portions, serial input data being distributed alternately between said shift register portions by the operation of a multiplexer, serial output data being obtained by picking up data alternately from said shift register portions by the operation of another multiplexer;

a transfer gate portion inserted between said random access memory portion and said shift register for carrying out parallel transfer, said transfer gate portion consisting of a plurality of groups of transfer gates for enabling selective connections of input and output terminals of each stages of said shift register portions either of the adjacent odd number bit line and even number bit line in said random access memory portion, said plurality of transfer gate groups being switched in correspondence with shift clock signals.

Fig. 1

Fig. 1A | Fig. 1B

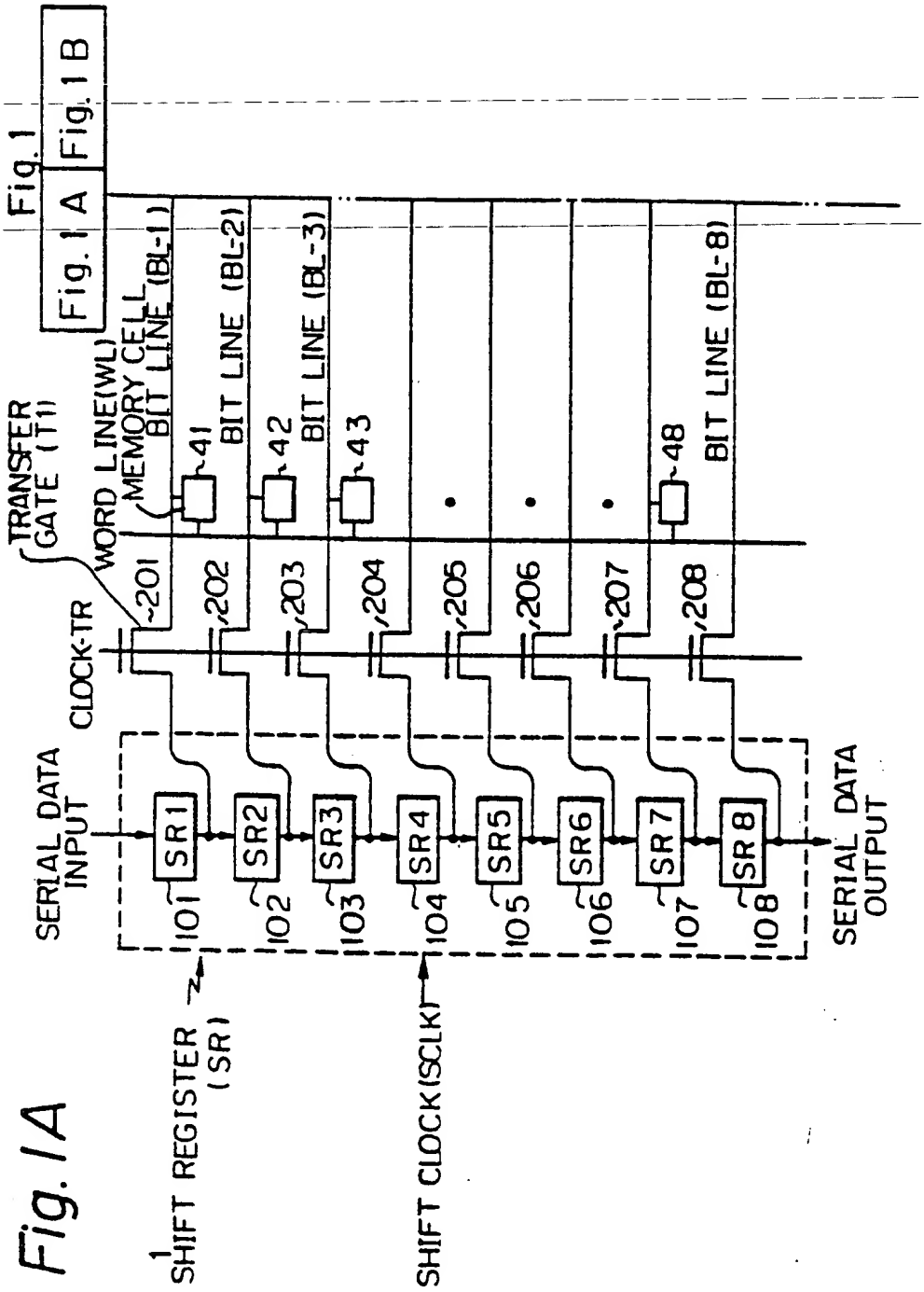


Fig. 1A

Fig. 1B

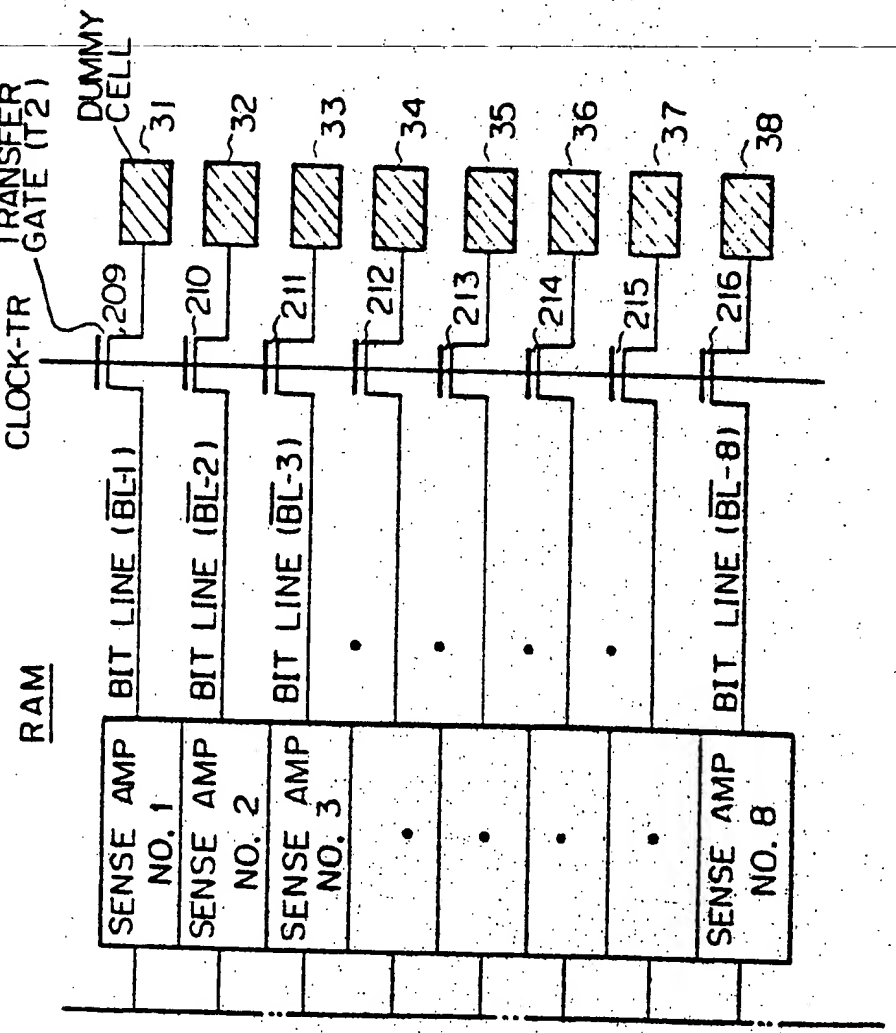

RAM
CLOCK-TR
TRANSFER GATE (T2)
DUMMY CELL
31
32
33
34
35
36
37
38
209
210
211
212
213
214
215
216
BIT LINE (BL-1)
BIT LINE (BL-2)
BIT LINE (BL-3)
BIT LINE (BL-8)
SENSE AMP NO. 1
SENSE AMP NO. 2
SENSE AMP NO. 3
SENSE AMP NO. 8

Fig. 2

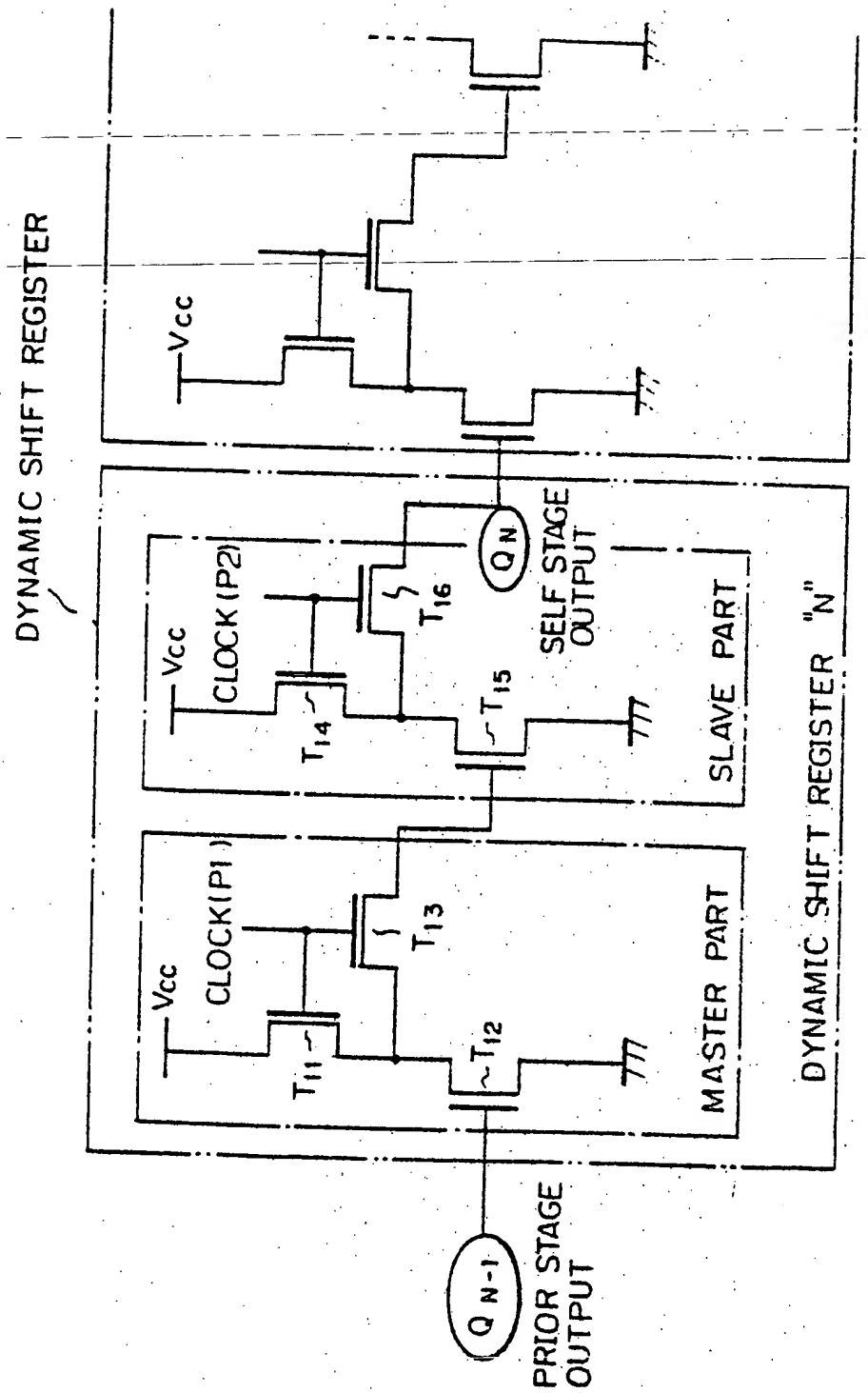

DYNAMIC SHIFT REGISTER
Vcc
CLOCK(P2)
T16
T14
T15
SELF STAGE OUTPUT
QN
SLAVE PART
CLOCK(P1)
T13
T11
T12
MASTER PART
DYNAMIC SHIFT REGISTER "N"
QN-1
PRIOR STAGE OUTPUT

Fig. 3

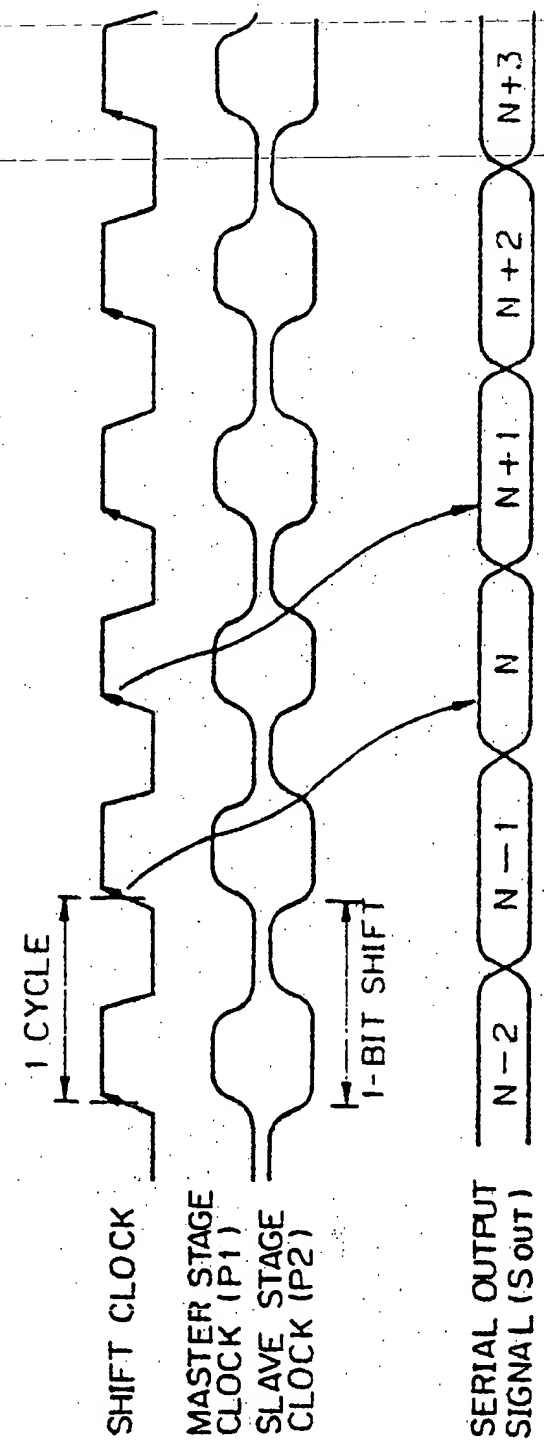

1 CYCLE
1-BIT SHIFT
SHIFT CLOCK
MASTER STAGE CLOCK (P1)
SLAVE STAGE CLOCK (P2)
SERIAL OUTPUT SIGNAL (Sout)
N-2
N-1
N
N+1
N+2
N+3

Fig. 4

Fig. 4 A	Fig. 4 B

Fig. 4 A

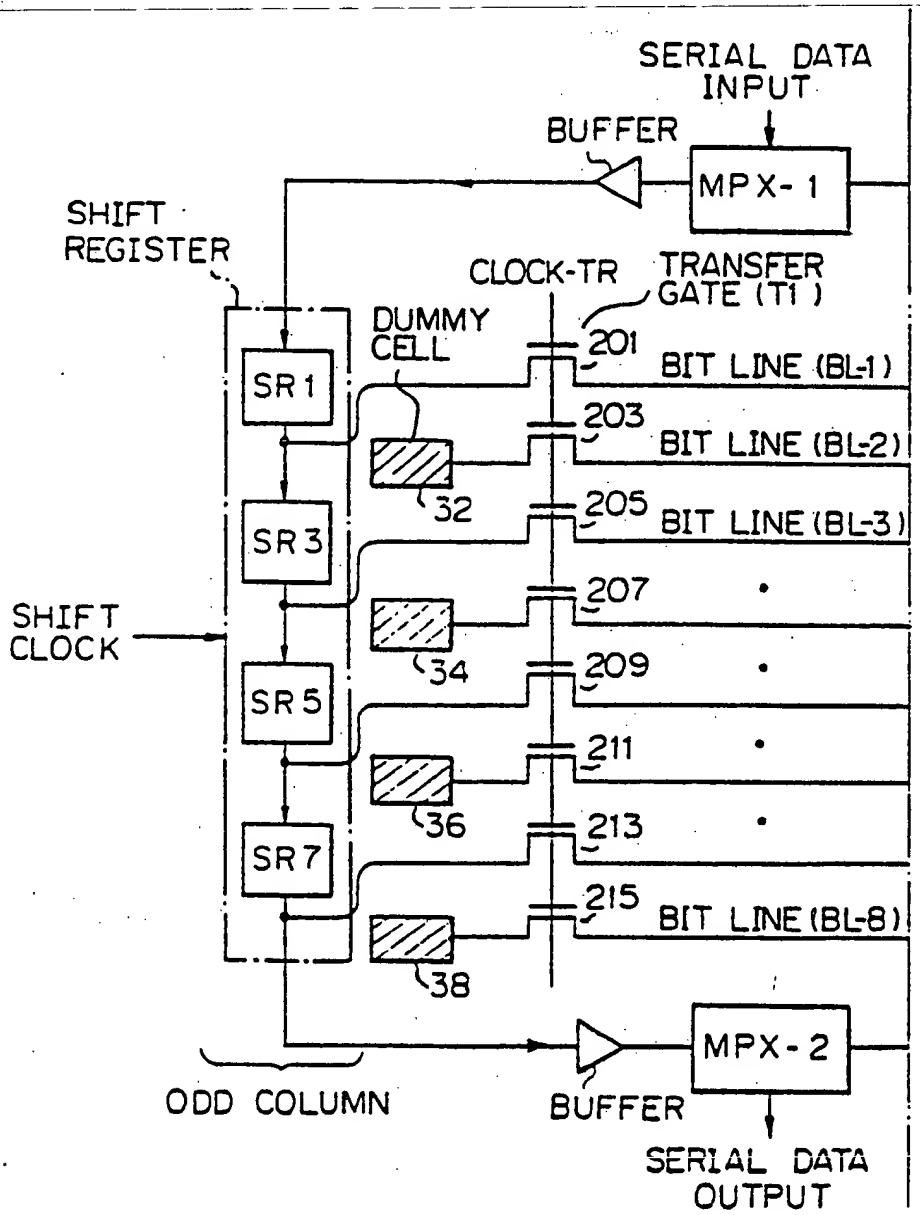


Fig. 4B

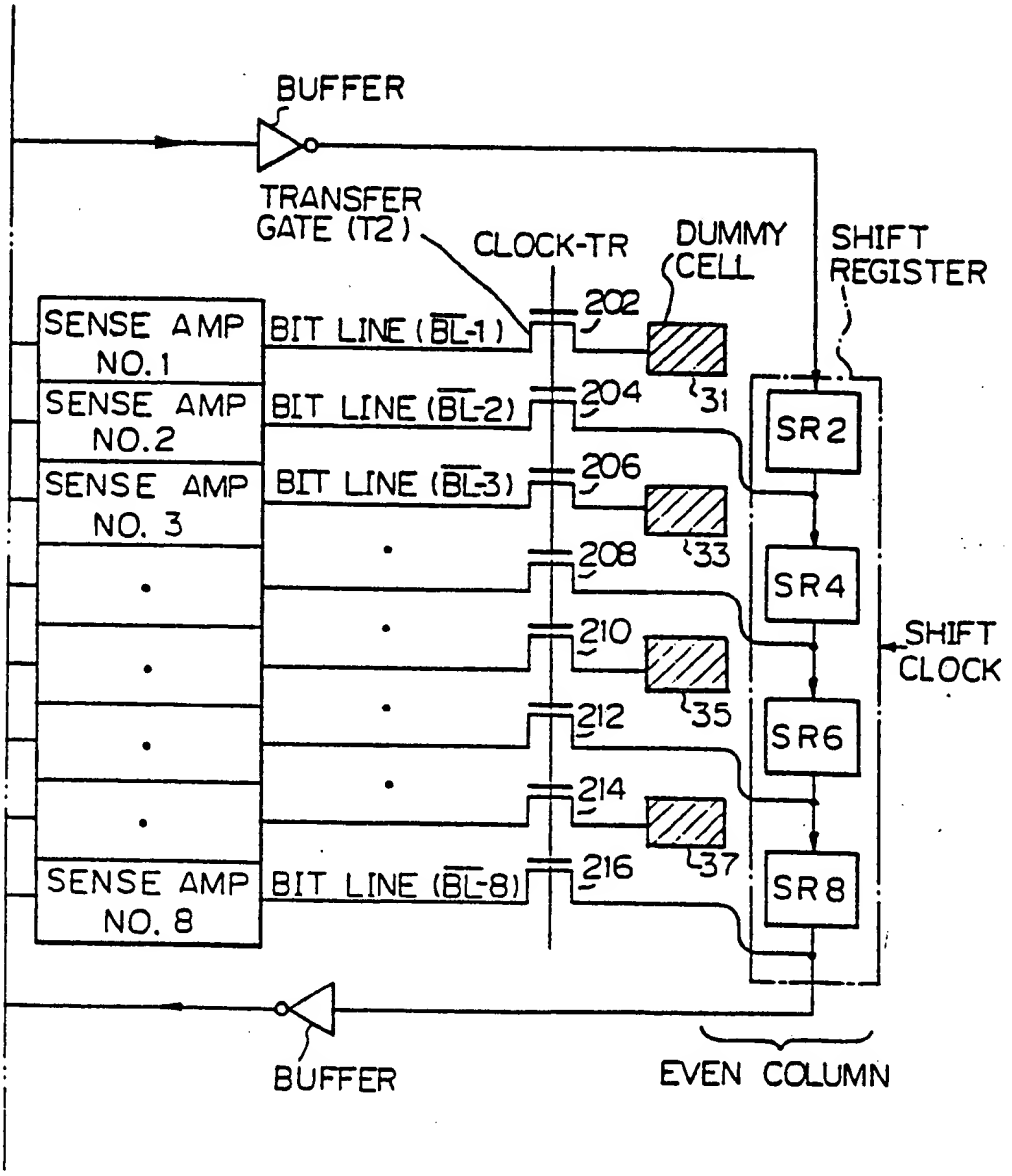
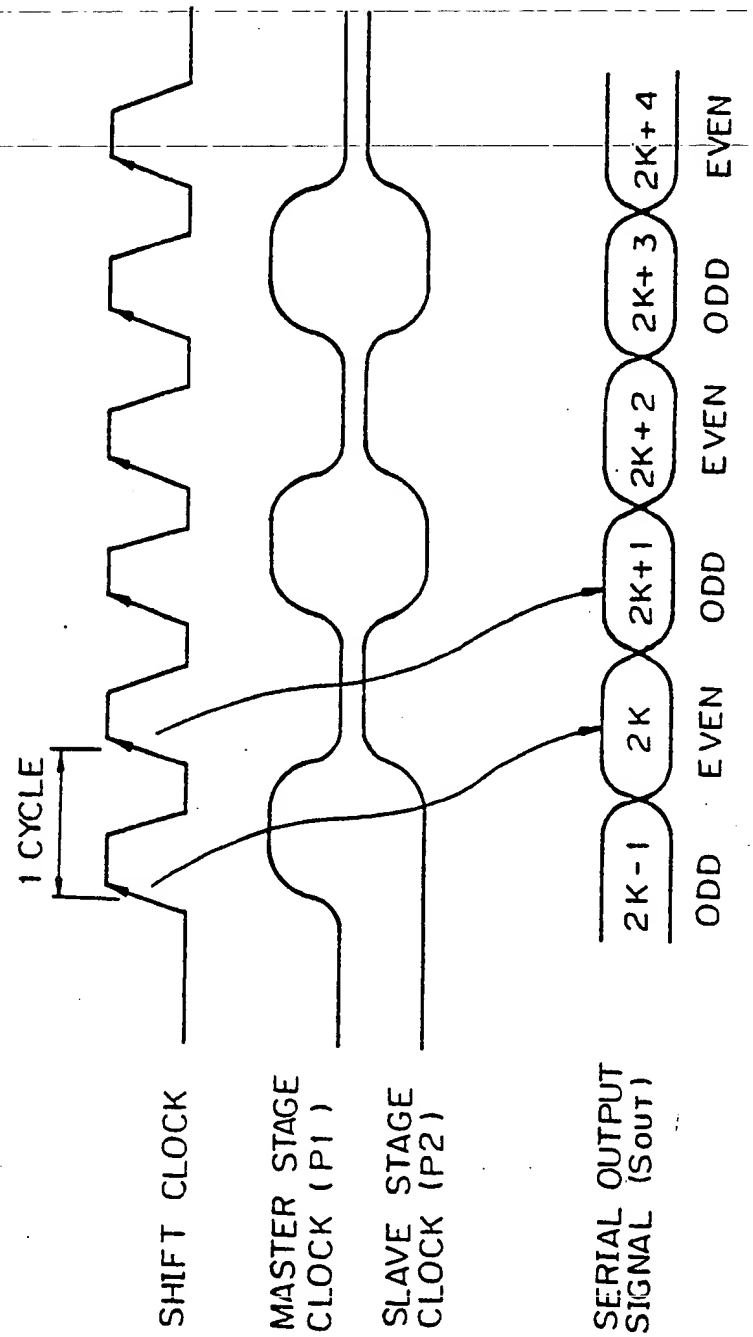

BUFFER
TRANSFER GATE (T2)
CLOCK-TR
DUMMY CELL
SHIFT REGISTER
SENSE AMP NO. 1
SENSE AMP NO. 2
SENSE AMP NO. 3
SENSE AMP NO. 8
BIT LINE (BL-1)
BIT LINE (BL-2)
BIT LINE (BL-3)
BIT LINE (BL-8)
202
204
206
208
210
212
214
216
31
33
35
37
SR2
SR4
SR6
SR8
SHIFT CLOCK
BUFFER
EVEN COLUMN

Fig. 5


1 CYCLE
SHIFT CLOCK
MASTER STAGE CLOCK (P1)
SLAVE STAGE CLOCK (P2)
SERIAL OUTPUT SIGNAL (SOUT)
2K-1
2K
2K+1
2K+2
2K+3
2K+4
ODD
EVEN
ODD
EVEN
ODD
EVEN

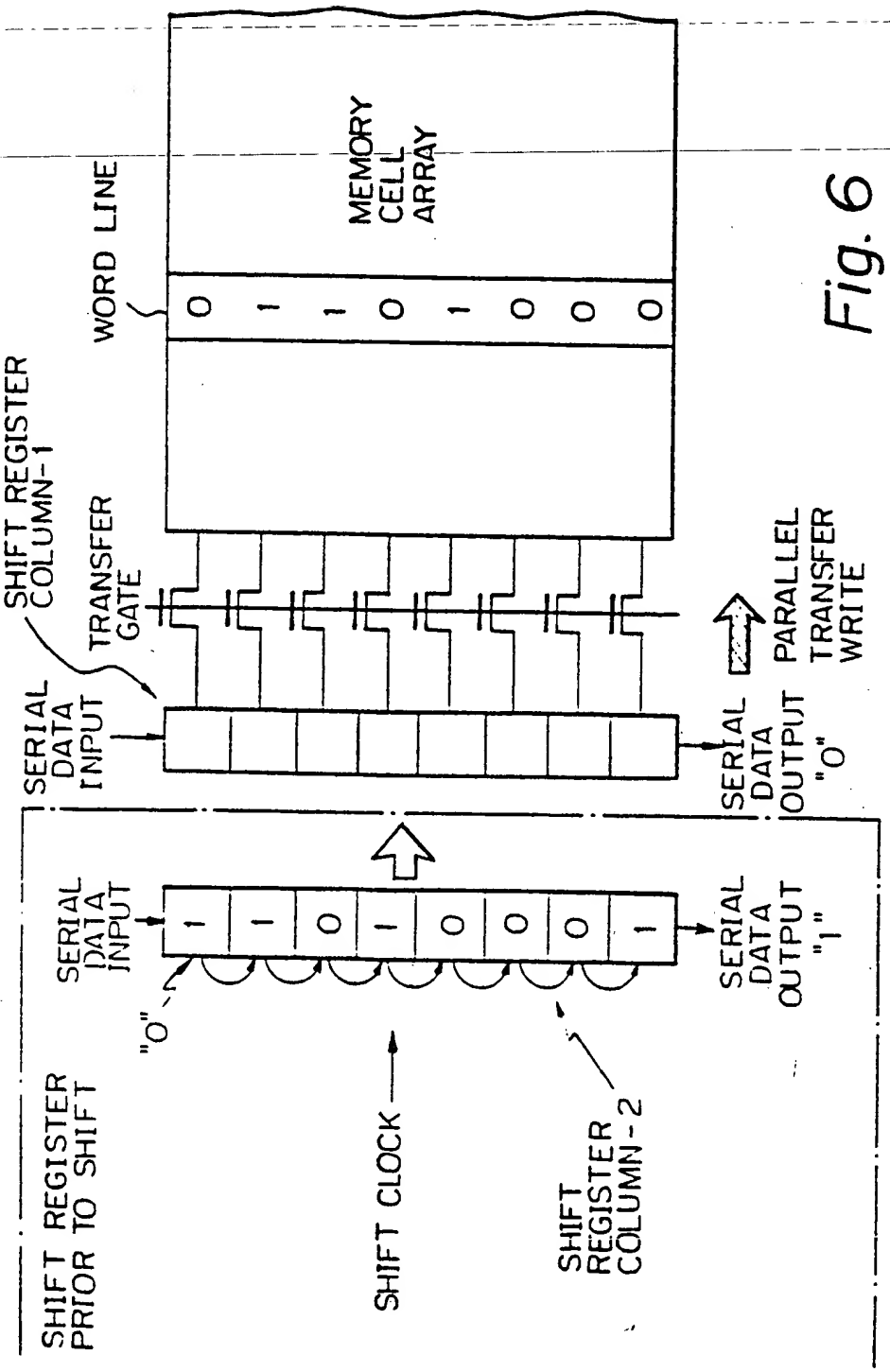

MEMORY CELL ARRAY
WORD LINE
0 1 1 0 1 0 0 0
SHIFT REGISTER COLUMN-1
TRANSFER GATE
SERIAL DATA INPUT
SERIAL DATA OUTPUT "0"
PARALLEL TRANSFER WRITE
SERIAL DATA INPUT
1 1 0 1 0 0 0 1
"0"
SERIAL DATA OUTPUT "1"
SHIFT REGISTER PRIOR TO SHIFT
SHIFT CLOCK
SHIFT REGISTER COLUMN-2

Fig. 6

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Fig. 7A

Fig. 7

Fig. 7A	Fig. 7B	Fig. 7C

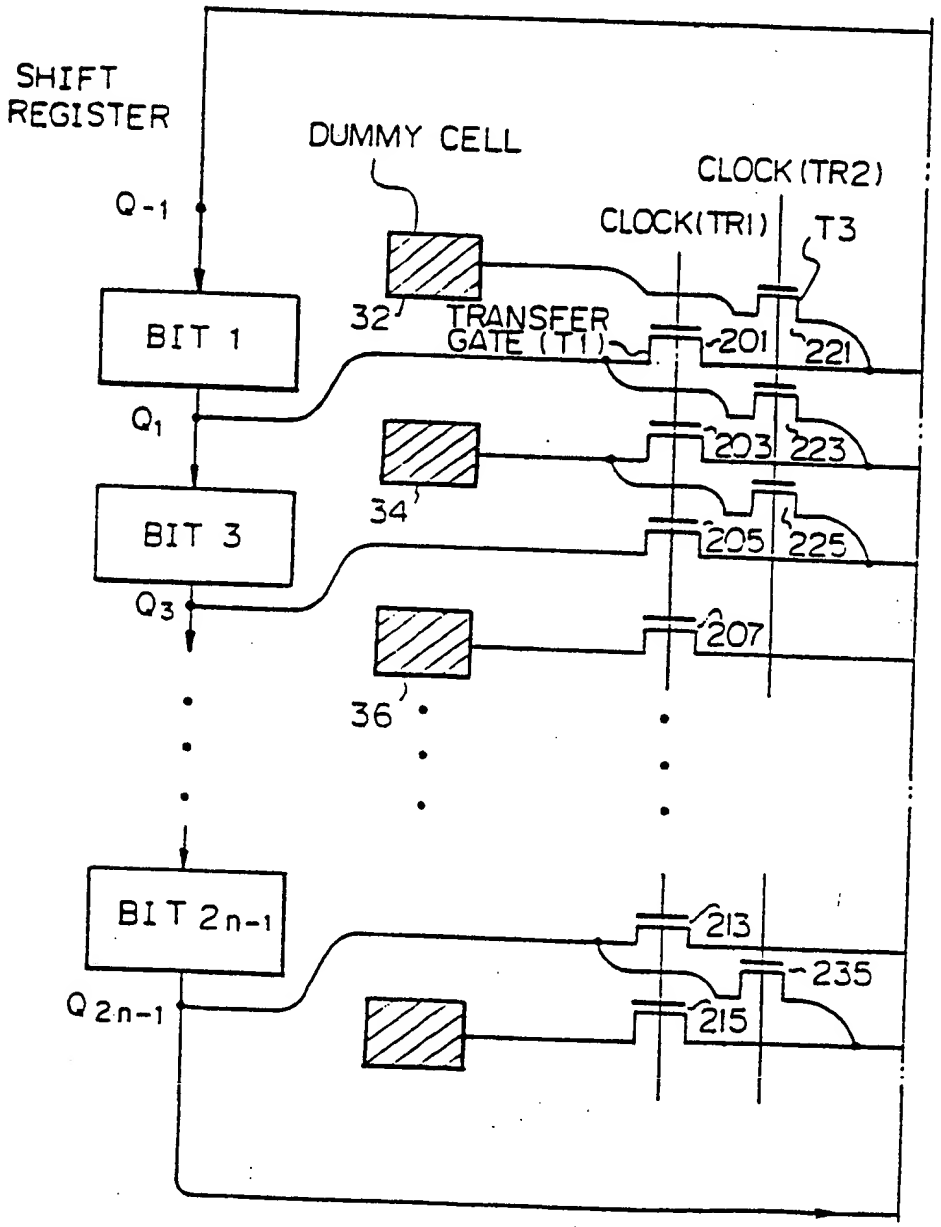


Fig. 7B

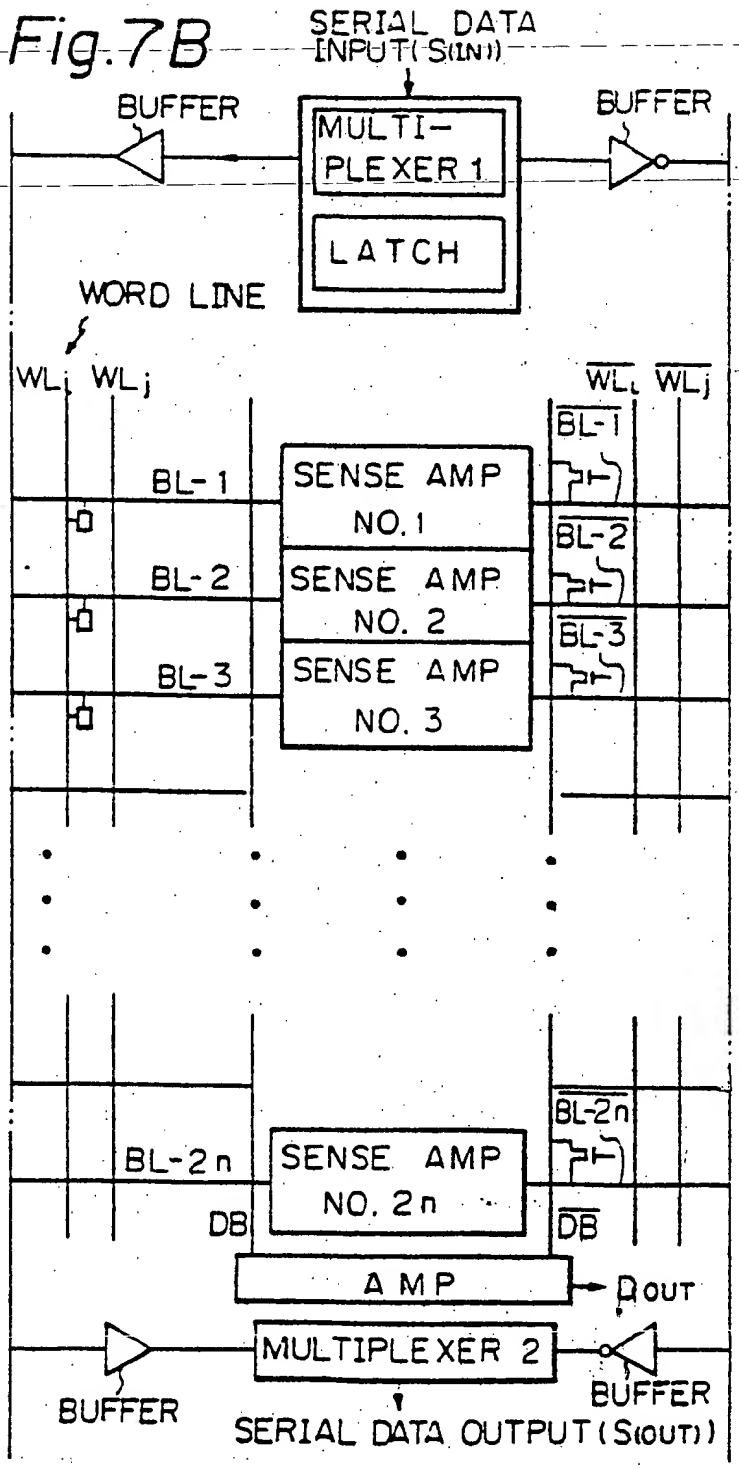

SERIAL DATA INPUT (S(IN))
BUFFER
MULTI-PLEXER 1
LATCH
BUFFER
WORD LINE
WLi
WLj
BL-1
BL-2
BL-3
SENSE AMP NO. 1
SENSE AMP NO. 2
SENSE AMP NO. 3
BL-2n
SENSE AMP NO. 2n
DB
AMP
Dout
MULTIPLEXER 2
BUFFER
BUFFER
SERIAL DATA OUTPUT (S(OUT))

Fig. 7 C

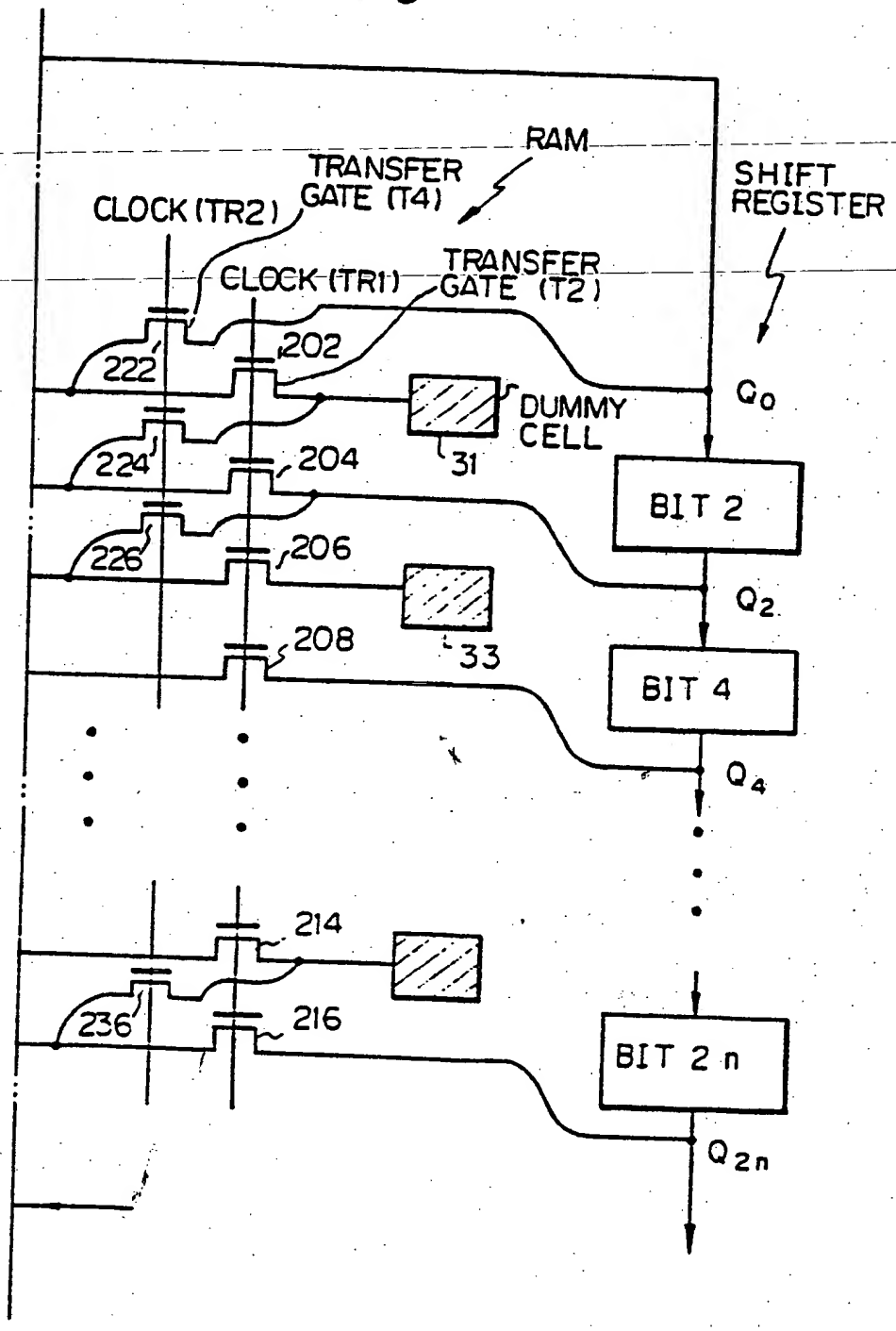

RAM
TRANSFER GATE (T4)
CLOCK (TR2)
CLOCK (TR1)
TRANSFER GATE (T2)
SHIFT REGISTER
222
202
224
204
226
206
208
214
236
216
DUMMY CELL
31
33
BIT 2
BIT 4
BIT 2 n
Q0
Q2
Q4
Q2n

Fig.8A

Fig. 8

Fig. 8A	Fig. 8B	Fig. 8C

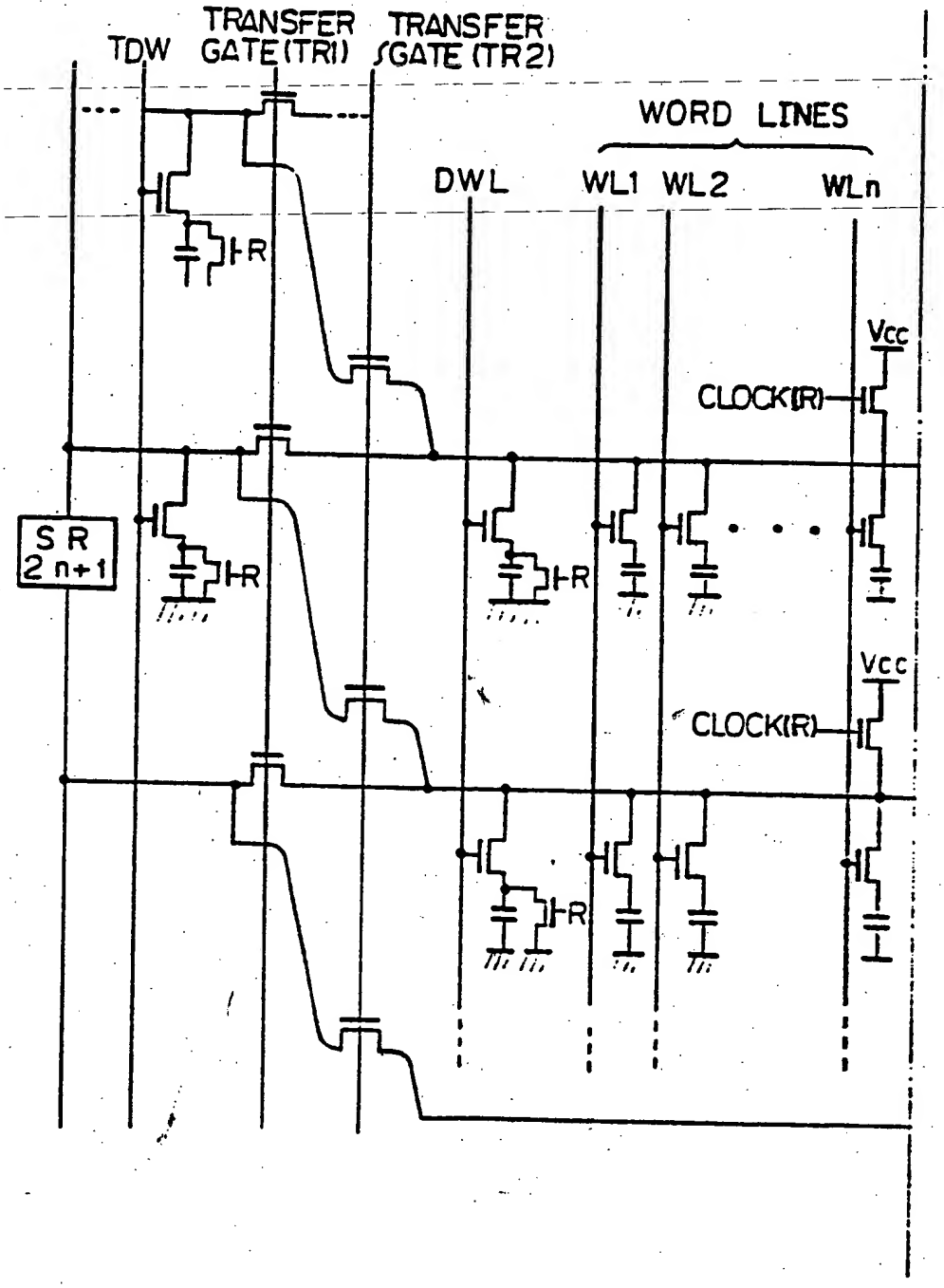


Fig. 8B

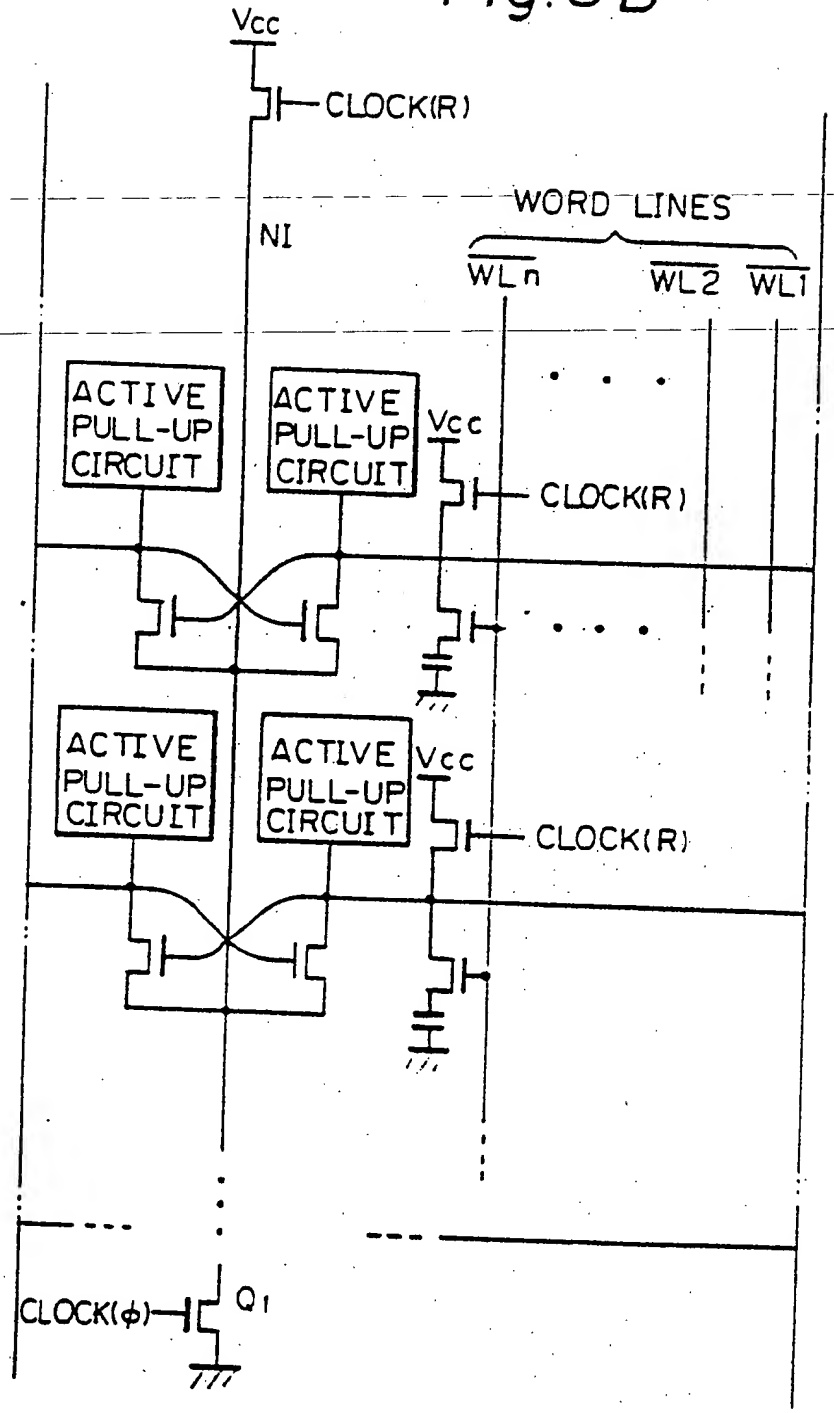

Vcc
CLOCK(R)
WORD LINES
NI
WLn
WL2
WL1
ACTIVE PULL-UP CIRCUIT
ACTIVE PULL-UP CIRCUIT
Vcc
CLOCK(R)
ACTIVE PULL-UP CIRCUIT
ACTIVE PULL-UP CIRCUIT
Vcc
CLOCK(R)
CLOCK(φ)
Q1

Fig. 8C

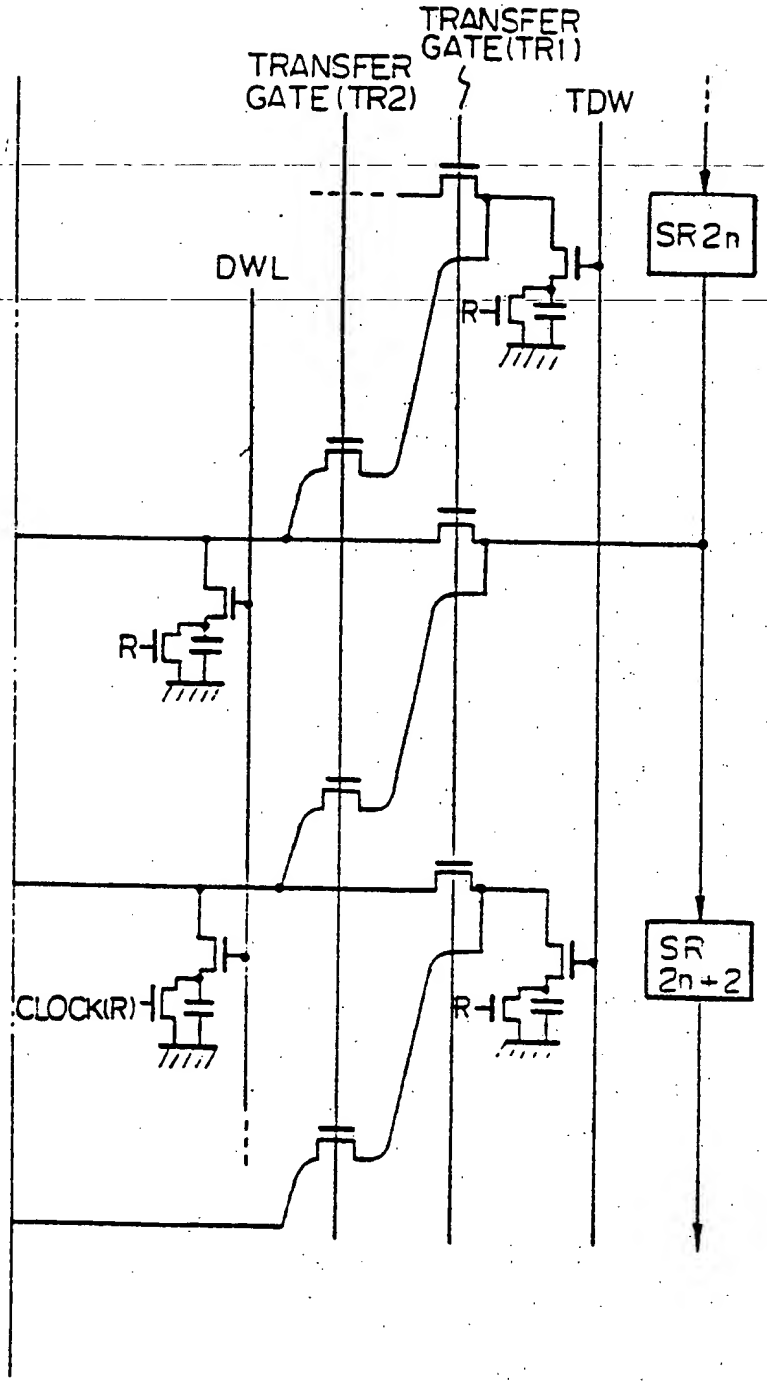

TRANSFER GATE(TR1)
TRANSFER GATE(TR2)
TDW
SR2n
DWL
R
R
CLOCK(R)
R
SR 2n+2

Fig. 9

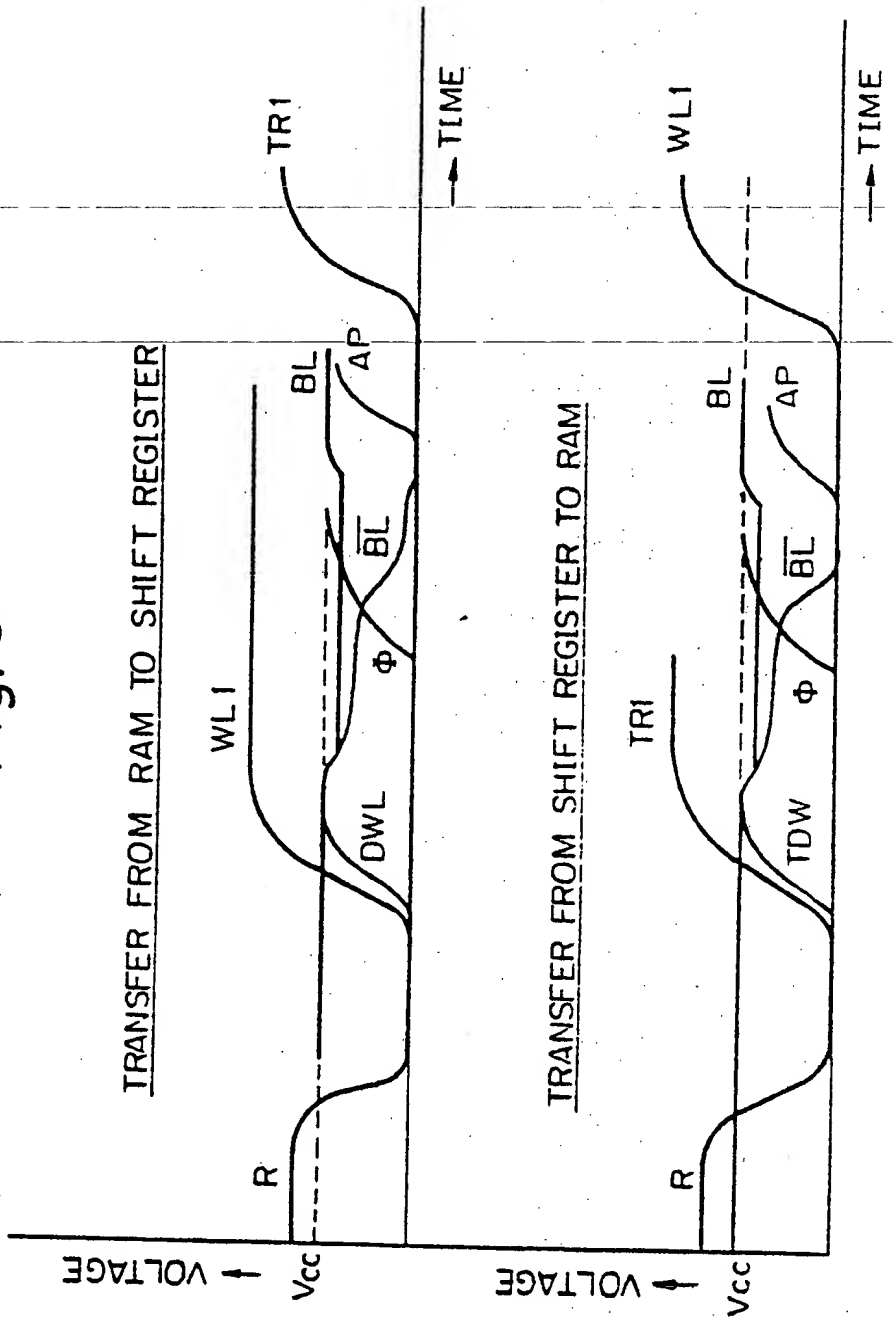

TRANSFER FROM RAM TO SHIFT REGISTER
WL1
TR1
BL
ΔP
$\overline{BL}$
Φ
DWL
R
Vcc
VOLTAGE
TIME
TRANSFER FROM SHIFT REGISTER TO RAM
WL1
TR1
BL
ΔP
$\overline{BL}$
Φ
TDW
R
Vcc
VOLTAGE
TIME

Fig. 10A

Fig. 10

Fig.10A	Fig.10B

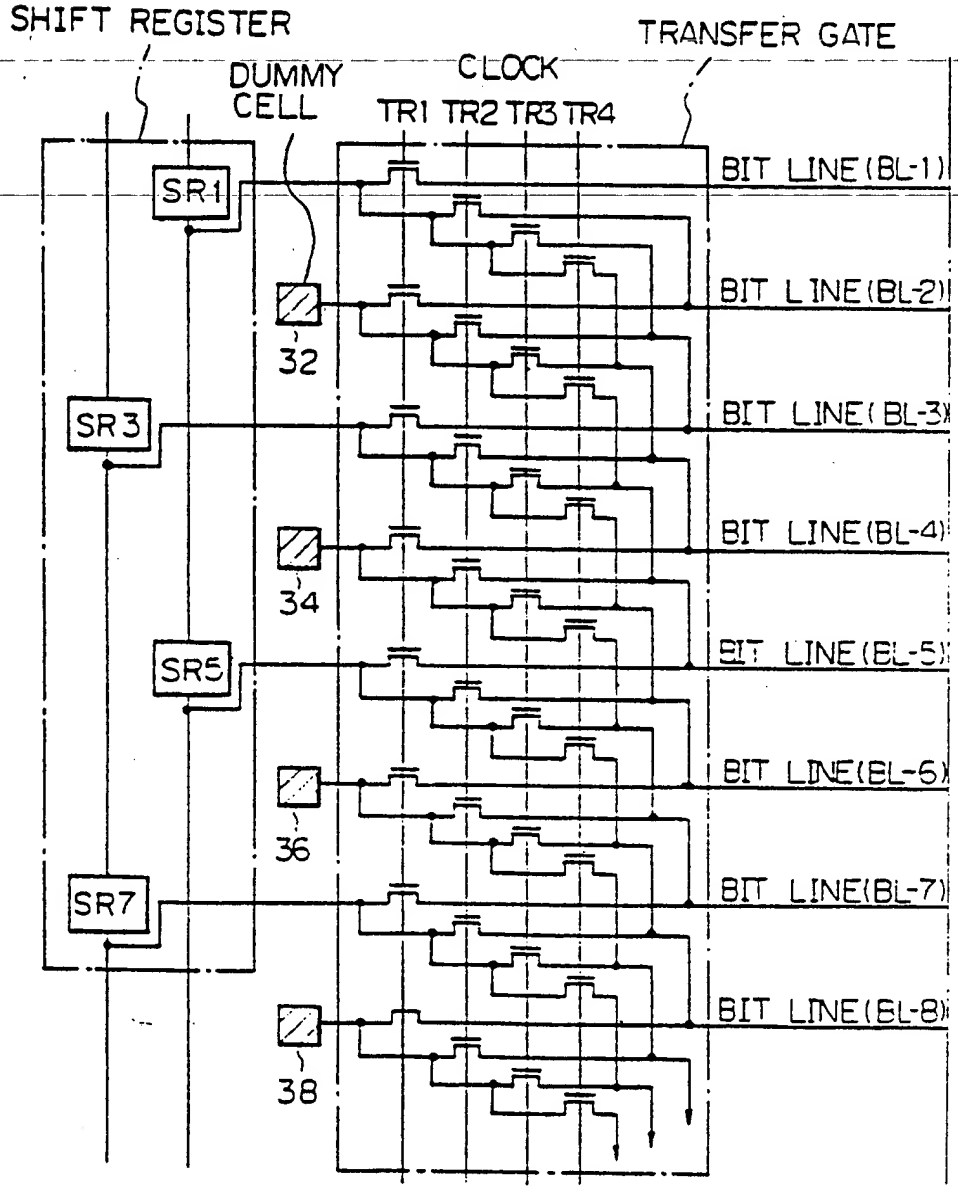
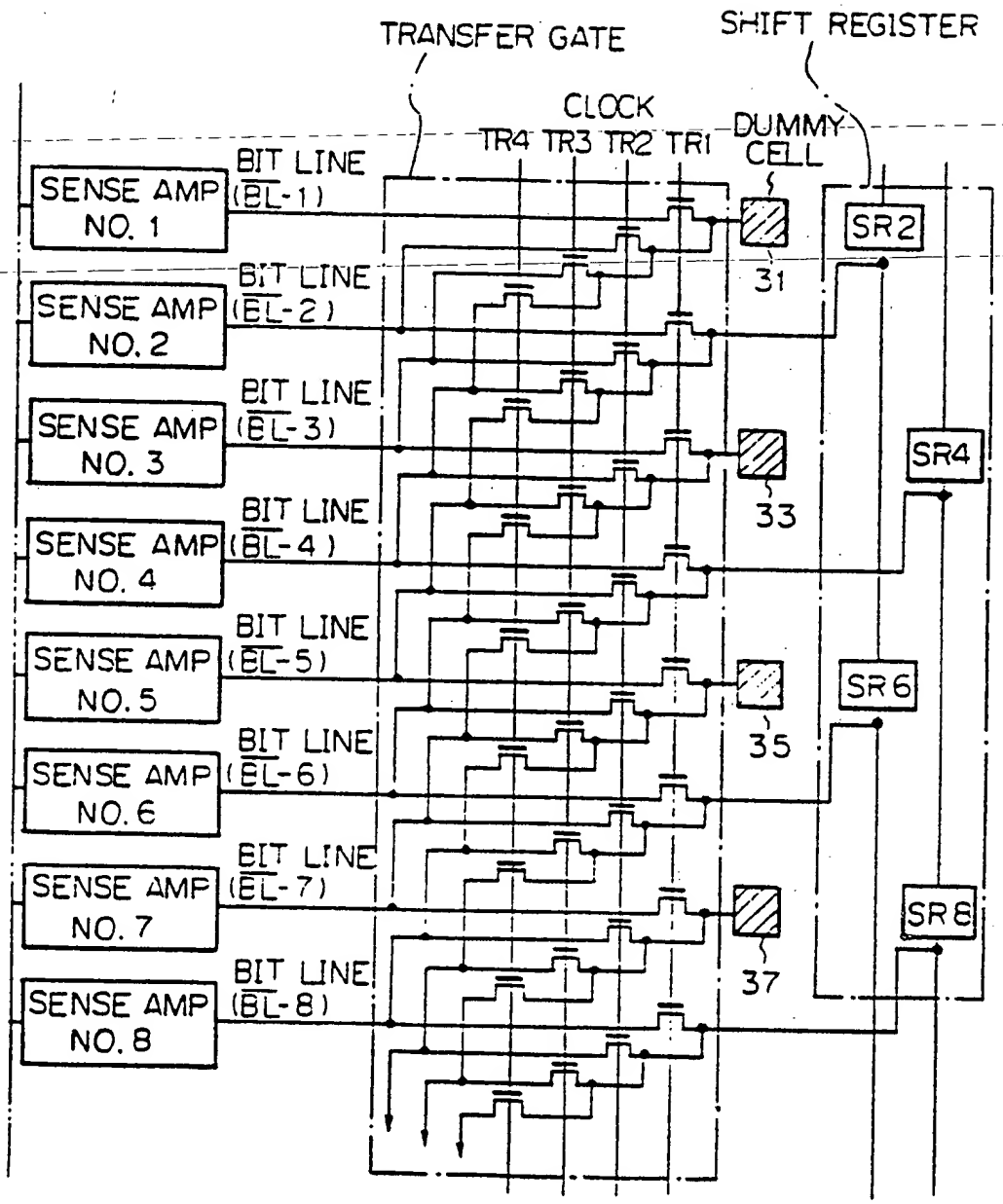


Fig. 10B


TRANSFER GATE
SHIFT REGISTER
CLOCK
TR4 TR3 TR2 TR1
DUMMY CELL
SENSE AMP NO. 1
BIT LINE (BL-1)
SENSE AMP NO. 2
BIT LINE (BL-2)
SENSE AMP NO. 3
BIT LINE (BL-3)
SENSE AMP NO. 4
BIT LINE (BL-4)
SENSE AMP NO. 5
BIT LINE (BL-5)
SENSE AMP NO. 6
BIT LINE (BL-6)
SENSE AMP NO. 7
BIT LINE (BL-7)
SENSE AMP NO. 8
BIT LINE (BL-8)
31
33
35
37
SR2
SR4
SR6
SR8